Q.P. Code: 16EC431 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech IV Year I Semester Regular & Supplementary Examinations Feb-2021

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Determine the relationship between I_{ds} and V_{ds} in Linear and Saturation region.	6M
	b	List the steps involved in n-well fabrication process.	6M
		OR	
2	a	Analyze the different types of alternative pull-ups with neat diagram.	6M
	b	Define Moore's law. Discuss the generations of integrated circuits.	6M

UNIT-II

3	a	Develop the schematic and layout for 2 input NAND gate.	8M
	b	Build the layout of AND-OR-INVERTER in NMOS design Styles.	4M
		OR	
4	a	What is a stick diagram? Design the stick diagram of a three- input CMOS NOR gate.	7M
	b	Explain 2μm based design rules with neat sketches.	5M

UNIT-III

5	a	Explain the following (i) Floor planning (ii) Routing.	6M
	b	Illustrate the Power delay estimation in VLSI circuits.	6M
		OR	
6	a	Explain Pseudo NMOS logic.	5M
	b	Illustrate the dynamic CMOS logic circuit with any one example.	7M

UNIT-IV

7	a	Explain Unsigned Magnitude Comparator with neat diagram.	6M
	b	Design and Explain Johnson Counter.	6M
		OR	
8	a	Explain about 4 transistor Dynamic memory cell.	6M
	b	Explain about different types of memory elements.	6M

UNIT-Voila 1.0

9	a	Discuss in detail about standard cell design with suitable diagrams.	6M
	b	Demonstrate the following i) I/O pads ii) SPLD iii) LUT	6M
		OR	
10	a	Design the logic diagram of PLA for the following. Y1=A'B'C'+ABC+A'B+ABC' Y2=ABC+A'B'C+AC Y3=A'BC'+AB'C+B'C'	6M
	b	Compare the PROM, PAL, and PLA.	6M

*** END ***